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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,031	12/30/2003	William H. Howland JR.	1880-031569	8283

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EXAMINER	
KOBERT, RUSSELL MARC	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,031	HOWLAND ET AL.	
	Examiner	Art Unit	
	Russell M Kobert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Eriguchi et al (6583640).

Eriguchi et al anticipates a method of determining a permittivity of a dielectric layer of a semiconductor wafer comprising:

(a) providing a means (Figures 3 and 4) for contacting a topside (3) of a semiconductor wafer (4), the contact means including at least a partially spherical surface (lower portion of 2) formed from a conductive material (col 9, ln 64-66; col 27, ln 8-18);

(b) determining a thickness of a dielectric layer on the semiconductor wafer having semiconducting material underlying the dielectric layer (col 10, ln 3-5);

(c) causing the topside of the semiconductor wafer to support the at least partially spherical surface of the contact means in spaced relation to the semiconducting material thereby defining a capacitor (col 4, ln 33-36; spaced relationship of the wafer, dielectric layer and the conductive bumps form a capacitor);

(d) applying an electrical stimulus to the contact means and the semiconducting material when the capacitor is defined (col 4, ln 36-37);

(e) determining a capacitance of the capacitor from the response thereof to the applied electrical stimulus (col 4, ln 41-53); and

(f) determining a permittivity (dielectric constant) of the dielectric layer as a function of the capacitance determined in step (e) and the thickness of the dielectric layer determined in step (b); (col 26, ln 39-61) as recited in claim 1.

Eriguchi et al anticipates a system for determining a permittivity of a dielectric layer of a semiconductor wafer comprising:

means (Figures 3 and 4) for contacting a topside (3) of a semiconductor wafer (4), the contact means including at least a partially spherical surface (lower portion of 2) formed from a conductive material (col 9, ln 64-66; col 27, ln 8-18);

means for determining a thickness of a dielectric layer on the semiconductor wafer having semiconducting material underlining the dielectric layer (col 10, ln 3-5);

means for moving the topside of the semiconductor wafer and the at least partially spherical surface of the contact means into contact thereby defining with the dielectric layer a capacitor (col 4, ln 33-36; spaced relationship of the wafer, dielectric layer and the conductive bumps form a capacitor);

means for applying an electrical stimulus to the contact means and the semiconducting material when the capacitor is defined (col 4, ln 36-37); and

means for determining from the response of the capacitor to the applied electrical stimulus a capacitance of the capacitor and for determining therefrom a

permittivity (dielectric constant) of the dielectric layer as a function of the capacitance and the thickness of the dielectric layer (col 4, ln 41-53 and col 26, ln 39-61); as recited in claim 7.

Eriguchi et al anticipates a method of determining a permittivity of a dielectric layer of a semiconductor wafer comprising:

(a) determining a thickness of the dielectric layer overlaying semiconducting material of a semiconductor wafer (col 10, ln 3-5);

(b) moving a topside of the semiconductor wafer and a spherical portion of an at least partially spherical and electrically conductive surface into contact (col 4, ln 33-36);

(c) applying an electrical stimulus between the electrically conductive surface and the semiconducting material (col 4, ln 36-37);

(d) determining from the applied electrical stimulus a capacitance of a capacitor comprised of the electrically conductive surface and the semiconducting material (col 4, ln 41-53; spaced relationship of the wafer, dielectric layer and the conductive bumps form a capacitor); and

(e) determining a permittivity (dielectric constant) of the dielectric layer as a function of the capacitance determined in step (d) and the thickness of the dielectric layer determined in step (a); (col 26, ln 39-61); as recited in claim 13.

The limitations of claims 2-6, 8-12 and 14-18 are considered inherent and within the operable scope according to Eriguchi et al.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Taylor et al (5528153), Kono et al (6037781) and Fauque (6220080) show measurement apparatus for determining permittivity of a dielectric layer of a semiconductor wafer.

4. A shortened statutory period for response to this action is set to expire three month(s) from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell Kobert whose telephone number is (571) 272-1963. The Examiner's Supervisor, Nestor R. Ramirez, can be reached at (571) 272-2034. For an automated menu of Tech Center 2800 phone numbers call (571) 272-2800.

Russell M. Kobert
Patent Examiner
Group Art Unit 2829
January 27, 2005

VINH NGUYEN
PRIMARY EXAMINER
A.U. 2829
01/31/05